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Analysis and hardware testing of cell capacitor discharge currents during DC faults in half-bridge modular multilevel converters

A.A.Aboushady*, K.H.Ahmed*, D.Jovcic*

** School of Engineering, University of Aberdeen, Aberdeen,UK, AB24 3UE*

Keywords: Cell capacitor discharge, DC faults, Driver level protection, Overcurrent protection.

Abstract

This paper focuses on the behaviour of the cell capacitor discharge currents during DC faults in half-bridge modular multilevel converters. Active switches, not designed for fault conditions, are tripped to minimize discharge currents effect on the semiconductor switches. Two levels of device protection are commonly in place; driver level protection monitoring collector-emitter voltage and overcurrent protection with feedback measurement and control. However, unavoidable tripping delay times, arising from factors such as sensor lags, controller sampling delays and hardware propagation delays, impact transient current shape and hence affect the selection of semiconductor device ratings as well as arm inductance. Analytical expressions are obtained for current slew rate, peak transient current and resultant *I2t* for the cell capacitor discharge current taking into account such delays. The study is backed by experimental testing on discharge of a 900V MMC capacitor.

1 Introduction

Modular multilevel converter (MMC) is the current state of the art in voltage source converter (VSC) HVDC technology. It has been a recent attractive area of research in addition to commercially attracting grid and utility companies such as the Trans Bay project already deployed in California and the near future Spain-France HVDC interconnect. It provides a modular approach to construct a reliable and cost effective AC voltage with increased number of levels. In addition to advantages of conventional two level VSCs, among the MMC main features are the possibility of continuously operating under unbalanced conditions, capability of surviving symmetrical and asymmetrical AC faults without increasing the risk of system collapse and possibility of complete DC fault isolation for some of its topologies [1-3].

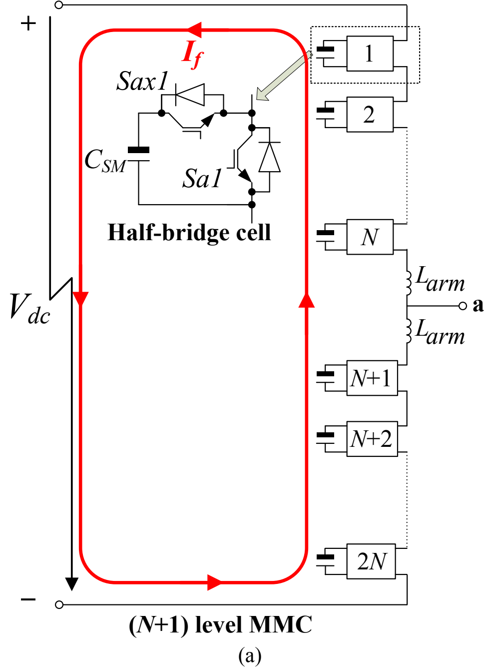
DC fault management with MMCs has been a subject of recent vigorous research [4-6]. In MMCs, DC fault currents comprise two main components, AC side current inrush and cell capacitor discharge current. During DC faults, full-bridge MMCs are tripped to block both current components feeding the fault, hence full-bridge MMC is a completely fault-tolerant structure. In half-bridge MMCs, semiconductor switch tripping stops cell capacitors discharging, while AC side current flow is uncontrollable. The latter is either bypassed using anti-parallel thyristors at cell level or allowed to pass through IGBT anti-parallel diodes until external breakers trip similar to two-level VSCs. This paper does not study the AC side current component since this is dependent on AC side circuit configuration. The main purpose of this paper is to focus on the effect of the cell capacitor discharge current component which flows in the active semiconductor switches in both half-bridge and full-bridge cells before tripping during DC faults. The study will be conducted using half-bridge MMC due to its simplicity, lower losses and lower footprint/cost compared to full-bridge cells.

Tripping the active switches after fault occurrence is not an instantaneous action. Inevitable delays arise from factors such as sensor lags, controller sampling delays and hardware propagation delays. During this period of extended current conduction, transient current shape is affected. Analytical expressions are derived for the current slew rate, peak transient current and resultant *I2t* to ensure semiconductor devices are adequately rated. MMC arm inductance can also be designed accordingly to limit this discharge current. The analytical study is backed with experimental testing on discharge of a 900V MMC capacitor.

For switch tripping to be realized during DC faults, two levels of device protection are commonly used; firstly software-based protection where overcurrent is detected with feedback measurement and control and secondly hardware based protection where IGBT collector-emitter voltage is monitored and used to trip switches. The final part of this paper shows how the two levels of protection interact and highlights their relative response in tripping the semiconductor devices.

2 Analysis of MMC cell capacitor discharge current

Fig.1(a) shows circuit diagram for (N+1) level single-phase MMC with half-bridge cells. The cell main and auxiliary switches are denoted by *Sa* and *Sax* respectively. By definition, at any instant in time N cells are conducting. When a pole-to-pole DC fault is applied at the DC terminals, a worst case scenario is assumed. This scenario is characterized by the sustained conduction of N auxiliary switches (*Sax*) until tripping to allow maximum cell capacitor discharge currents. Fig.1(b) shows the MMC phase leg equivalent circuit with such scenario; I_f and R_f being the fault current and resistance respectively, I_{sa} and I_{Sax} are main and auxiliary switch currents, C_{eq} is the equivalent cell capacitance due to N series cell capacitances C_{SM}, V_{eq} is the voltage on the equivalent capacitance C_{eq} and L_{arm} is the MMC arm inductance. This section will be divided into analysis of two periods; auxiliary switch *Sax* conduction (before tripping) and main switch (diode) *Da* conduction (after tripping).



(a)

(b)

Fig.1: (N+1) level MMC with pole-to-pole DC fault (a) Full circuit diagram, (b) Reduced equivalent circuit.

2.1 Auxiliary switch conduction

Fig. 2 shows the conduction path during the period after the fault trigger and before auxiliary switch *Sax* is tripped open. The analysis assumes the worst case scenario of continuous conduction (no on/off switching) during this period for the highest possible capacitor discharge current. The cell capacitances discharge through *Sax*. Circuit parasitic resistances are defined as

- R_{arm}: Arm inductance parasitic resistance
- R_{ceq}: Total equivalent ESR of C_{eq}
- R_{Sax}: On state resistance of auxiliary switch *Sax*

Total equivalent resistance is defined as

$$R_1 = 2R_{arm} + R_{Ceq} + R_{Sax} + R_f \tag{1}$$

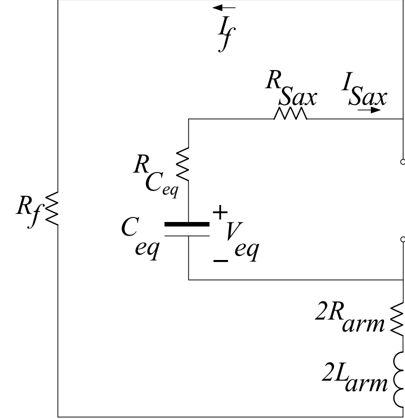


Fig.2: Equivalent circuit for period after fault trigger and before auxiliary switch tripping.

The second order dynamic equations of the circuit can be expressed as

$$V_{eq} = R_1 I_{Sax} + 2L_{arm}\frac{dI_{Sax}}{dt} \tag{2}$$

$$0 = I_{Sax} + C_{eq}\frac{dV_{eq}}{dt} \tag{3}$$

The two state variables are the auxiliary switch current I_{Sax} and equivalent capacitor voltage V_{eq}. Solving these two equations yields time domain expressions with initial conditions $I_{Sax}(0)=0$ and $V_{eq}(0)=V_{dc}$; where V_{dc} is the MMC DC link nominal voltage

$$I_{Sax}(t) = Ae^{-t/\tau}\sin Bt \tag{4}$$

$$V_{eq}(t) = V_{dc}e^{-t/\tau}\cos Bt + AR_1 e^{-t/\tau}\sin Bt \tag{5}$$

where

$$A = \frac{2V_{dc}C_{eq}}{\sqrt{8L_{arm}C_{eq} - R_1^2 C_{eq}^2}},\ B = \frac{\sqrt{8L_{arm}C_{eq} - R_1^2 C_{eq}^2}}{4L_{arm}C_{eq}},\ \tau = \frac{4L_{arm}}{R_1}$$

The following parameters can be deduced from (4) and (5)

A. Current slew rate

Initial rate of current rise can be calculated by

$$\left.\frac{dI_{Sax}}{dt}\right|_{t=0} = \frac{V_{dc}}{2L_{arm}} \tag{6}$$

Equation (6) provides an important design criterion for MMC arm inductance. According to (6), L_{arm} would be selected to meet maximum semiconductor slew rate (A/µs) requirements.

B. Peak current

According to how fast the auxiliary switch *Sax* is tripped open, the value of the peak current is determined. The absolute peak current I_{max} is obtained if the semiconductor switch did not trip or it tripped after a long time

$$\frac{dI_{Sax}}{dt} = 0$$
$$I_{\max} = \frac{V_{dc}R_1 C_{eq}}{4L_{arm}} e^{-T_{\max}/\tau} \tag{7}$$

where T_{max} defines the time interval after the fault at which absolute peak current occurs as shown in Fig. 3.

$$T_{\max} = \frac{1}{B}\tan^{-1} B\tau \tag{8}$$

It is important to mention If the semiconductor switch trip delay time T is less than T_{max}, then the peak tripping current will be less than the absolute peak current I_{max}.

C. Auxiliary switch thermal energy dissipation (I2t)

The thermal energy developed in the auxiliary switch *Sax* by the current pulse from the cell capacitor discharge is measured using the *I2t* parameter. This is an important factor as absolute switch ratings must satisfy the maximum possible energy dissipation during DC faults. Maximum *I2t* is obtained in case of no or delayed semiconductor switch tripping such that the cell capacitor fully discharges and the switch conducts absolute peak current I_{max}. In light of (4) and (8), maximum *I2t* can be calculated as follows

$$\left(I2t_{\max}\right)_{Sax} = \int_0^{T_{\max}} I_{Sax}^{\ 2}(t)\ dt$$

$$= \frac{A^2B^2\tau^3\left(1+B^2\tau^2-\left(5+B^2\tau^2\right)e^{-\frac{2T_{\max}}{\tau}}\right)}{4\left(1+B^2\tau^2\right)^2} \tag{9}$$

From semiconductor device manufacturer datasheet, absolute maximum ratings for current slew rate (A/µs) and maximum *I2t* can be obtained and hence used for selecting the MMC arm inductance L_{arm} to meet specifications in (6) and (9). The simplest method would be to start with (6) and obtain L_{arm}, then substitute the obtained L_{arm} in (9) to verify if it meets manufacturer specification for semiconductor device maximum *I2t*. It is worth noting that during DC side fault, auxiliary switch *Sax* does not provide a path for AC side current and the sole component of current in this switch is that arising from the cell capacitor discharge. Since the device cooling hardware is designed to appropriately remove the thermal energy developed in *Sax* during rated power operation, it therefore means that the calculated maximum *I2t* in (9) is the sole extra component of heat energy that needs to be catered for in assessing the predicted switch temperature rise, and hence the necessary additional cooling required.

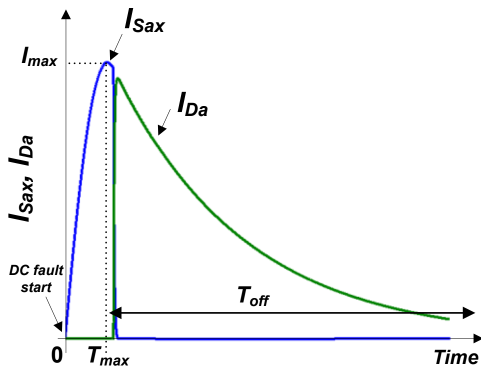


Fig.3: Auxiliary switch *Sax* and main diode (Da) currents during DC side fault assuming long tripping delay to allow for full cell capacitor discharge and absolute maximum current conduction.

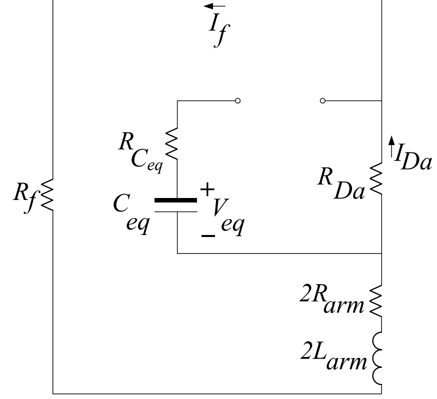


Fig.4: Equivalent circuit for period of main switch (diode) conduction.

2.2 Main switch (diode) conduction

Fig. 4 shows the conduction path after switch *Sax* has been tripped. There is no current path through the cell capacitor and arm inductor current can only conduct through the anti-parallel diode *Da*. In case of auxiliary switch *Sax* is not tripped or tripping delay time *T* is long, diode *Da* conduction is triggered when it is forward-biased by the voltage from the parallel conducting branch of the cell capacitor becoming lower than diode pick up threshold. This happens when the cell capacitor is fully discharged.

In this period, total circuit equivalent resistance is reduced and is defined as R_2 (R_2<R_1)

$$R_2 = 2R_{arm} + R_{Da} + R_f \tag{10}$$

This is a first order system with the following dynamic equation

$$0 = R_2 I_{Da} + 2L_{arm}\frac{dI_{Da}}{dt} \tag{11}$$

The diode current initial condition is the final current of the previous stage. This is dependent upon tripping delay time *T* and can be obtained by substituting for $t=T$ into $I_{Sax}(t)$ in (4).

$$I_{Da}(0) = I_{Sax}(t)\big|_{t=T} = Ae^{-T/\tau}\sin BT \tag{12}$$

Time-domain expression for diode current can therefore be obtained as

$$I_{Da}(t) = \left(Ae^{-T/\tau}\sin BT\right)e^{-\frac{R_2}{2L_{arm}}t} \tag{13}$$

The diode current is illustrated in Fig. 3. To calculate the maximum thermal energy *I2t* developed in the diode *Da* due to the cell capacitor discharge current component, substitute in (13) with $T=T_{max}$

$$\left(I2t_{\max}\right)_{Da} = \int_0^{T_{off}} I_{Da}^{\ 2}(t)\ dt$$

$$= \frac{A^2B^2\tau^2}{1+B^2\tau^2}\left(\frac{L_{arm}e^{-\frac{2T\max}{\tau}}}{R_2}\right)\left(1-e^{-\frac{R_2T_{off}}{L_{arm}}}\right) \tag{14}$$

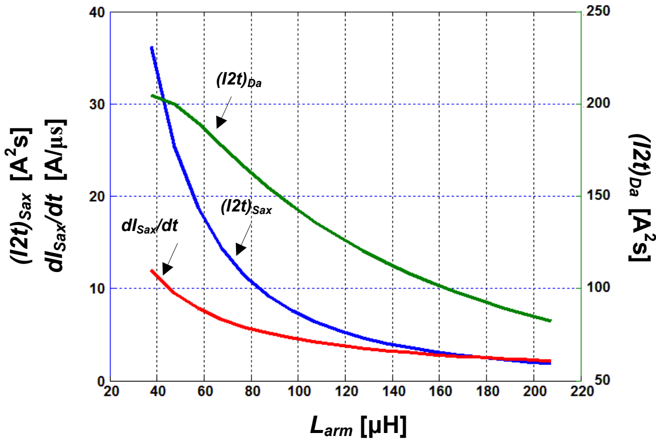


Fig.5: The effect of the MMC arm inductance value on various parameters related to cell capacitor discharge current during DC side faults.

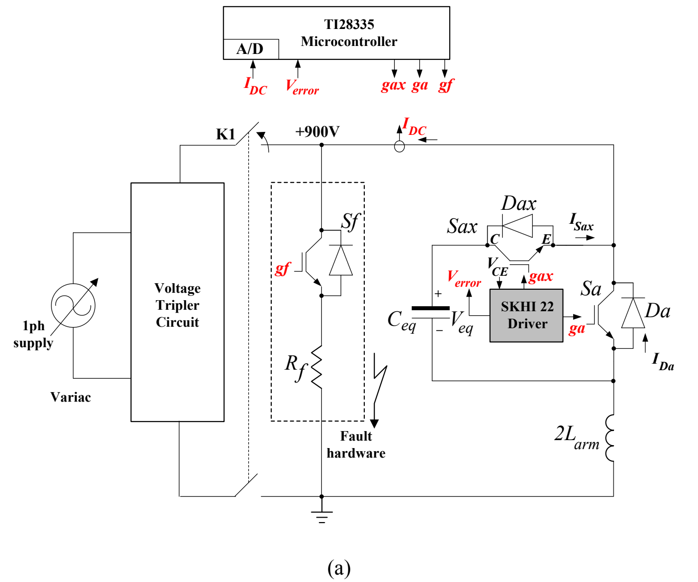
During DC side fault, half-bridge MMC diode *Da* conducts both fault current components; the decaying cell capacitor discharge current in addition to the AC side current component. However, in practice *Da* is bypassed externally at cell level by another protection switch that can withstand the high surge current from the AC side. For *Da* to conduct this current, fault tolerant VSC configuration has to be used such as the LCL-VSC [7] where an LCL circuit is designed at the AC side to confine DC fault current to twice rated current, which is generally tolerable by semiconductor switches. The analysis in this paper considers the case where fault tolerant half-bridge MMC is used. Therefore, the additional thermal energy developed in *Da* during the fault is from increased AC side current and from the decaying cell capacitor discharge current. Equation (14) calculates the latter component solely. For appropriate device cooling arrangements, both components need to be considered. However, it has been stated that the scope of this paper is the study of cell capacitor discharge only.
For a fixed tripping delay time *T*, Fig.5 illustrates how changing the value of MMC arm inductance L_{arm} affects cell capacitor discharge current slew rate, thermal energy developed in *Sax* and diode *Da*. The higher is the inductance the lower is the energy dissipated by the switches due to the delay in fault current rise introduced. This means that if the aggregate delay time (from sensor lag, propagation delays and controller sampling delays) is known to be *T*, delaying the current rise rate would reduce the energy build up in the switches during this time interval.

3 Semiconductor device overcurrent protection

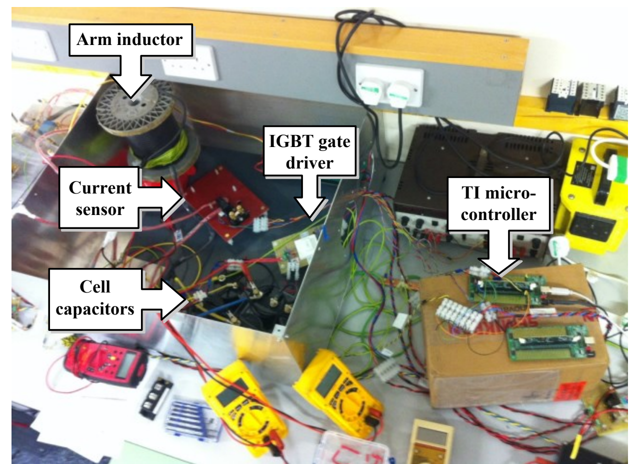
This section focuses on the main physical cause of the semiconductor switches tripping delay time *T* upon which the analysis in section 2 has been based. In order to protect the switches from overcurrent, typically two levels of protection exist; protection at device level and protection at system control level. The device level protection operates in hardware by flagging an error signal at the switch gate driver that trips the IGBT open when collector-emitter voltage exceeds a pre-set level due to overcurrent. This is named as V_{CE} monitoring and is typically triggered when V_{CE} exceeds 4-5V. Device protection at system control level is implemented by feedback controller depending on overcurrent sensing. The two levels of protection provide backup for each other to prevent switch destruction. Feedback protection with overcurrent sensing is associated with sensor lag, hardware propagation delays and microcontroller sampling delay. The effect and interaction of both protection methods are studied experimentally on discharging a 900V MMC cell capacitor.

3.1 Hardware testing setup

Fig.6 shows the experimental setup implemented and table 1 summarizes the components used. As shown in Fig.6(a), K1 is initially closed with *gf*=0, *gax*=1 and *ga*=0, to charge cell capacitor through input voltage supply. A voltage tripler circuit is used to step up input the 240V AC mains to 900VDC. Once capacitor is charged up, K1 is opened to isolate input supply circuit. Fault hardware is then triggered (*gf*=1) to initiate cell capacitor discharge which continues until protection logic trips cell IGBT.



(a)



(b)

Fig.6: Experimental test rig (a) circuit diagram, (b) photo.

Element	Value
C_{eq}	75 µF
L_{arm}	37.5 µH
R_f	100 mΩ
Sax and *Sa*	Semikron SKM145GB174DN 1700V, 100A
IGBT module driver	Semikron SKHI 22B

Table 1: Experimental component values

3.2 Experimental results

Firstly, driver level protection with V_{CE} monitoring only is applied to the circuit. The V_{CE} setting at switch trips is realised using an RC circuit configuration. The relationship between the V_{CE} setting and the IGBT tripping current is depicted in Fig.7. Actual tripping current is recorded from testing and compared with that from output characteristics in the IGBT manufacturer datasheet. Tripping currents obtained from experiment are marginally higher than datasheet values due to RC circuit natural response and inherent driver circuit propagation delays.

Secondly, overcurrent protection is implemented solely by sensing switch current and using feedback control to trip IGBT once current exceeds a pre-set threshold. Fig.8 shows the actual tripping currents for overcurrent protection compared to threshold settings applied. Ideal protection would be to trip the switch exactly at the threshold setting, but in practically this is not achievable due to accumulated delays arising from the current sensor, hardware circuitry propagation delays in addition to the microcontroller sampling delay introduced when sampling the measured current. Fig.8 also shows the relationship between the threshold setting and actual tripping current for the driver level protection which can be obtained from the results in Fig.7. The comparison between both methods of protection shows that tripping currents are higher with the feedback controller due to the longer delays associated with this method of protection. The main reason for this is that in overcurrent protection the signal is processed through more stages before switch tripping action is taken compared to driver level protection which occurs more or less instantly at switch level.

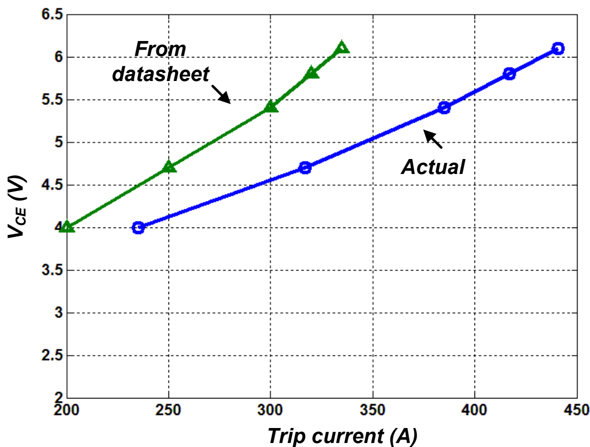


Fig.7: Relationship between collector-emitter voltage setting including manufacturer setting (from datasheet) and actual tripping current.

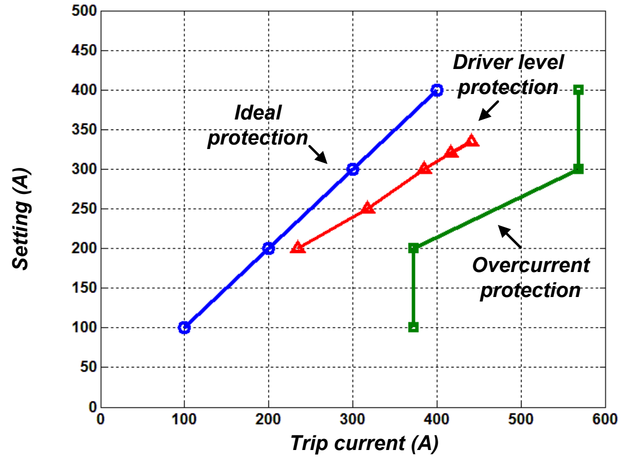
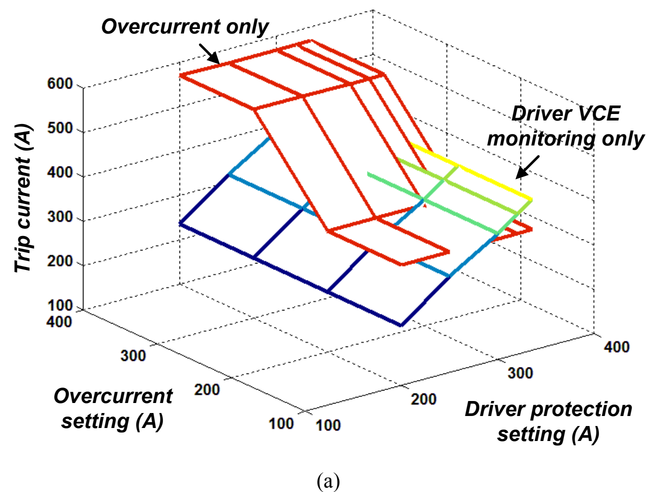
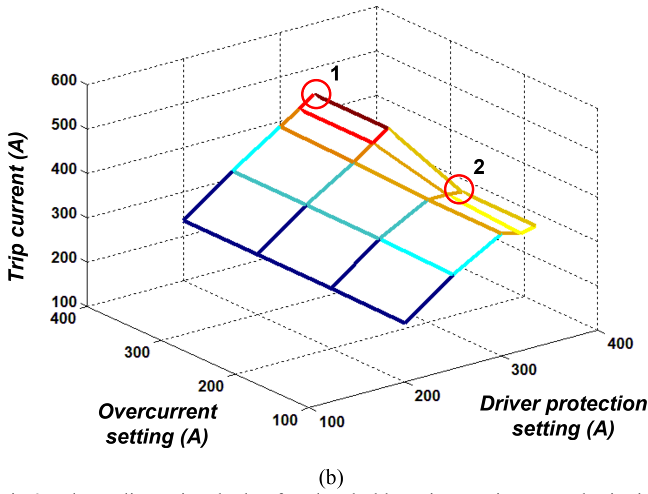


Fig.8: Relationship between threshold setting and actual tripping currents for both methods of protection compared to ideal case.

Fig.9(a) depicts the relationship between threshold setting and actual tripping currents for both methods of protection (illustrated in Fig.8) in a three dimensional plot. This describes the interaction between both methods and how they are expected to behave when applied simultaneously. Their interlinked behaviour is derived such that for every possible combination of both protection methods threshold settings, the method providing the lower tripping current is selected. The resulting plane is shown in Fig.9(b). The figure confirms that driver level protection is predominantly first to flag and is in operation most of the time. Overcurrent protection with feedback control is only in operation when driver threshold setting is high enough compared to overcurrent threshold setting. The difference compensates for the longer feedback and sampling delays, hence allowing overcurrent protection to trip IGBT before driver protection. However, in practical it is highly unlikely to have the two current settings highly different which conclude that driver level protection is most commonly faster to trip IGBTs. Feedback overcurrent protection provides the backup in case of driver protection failure.



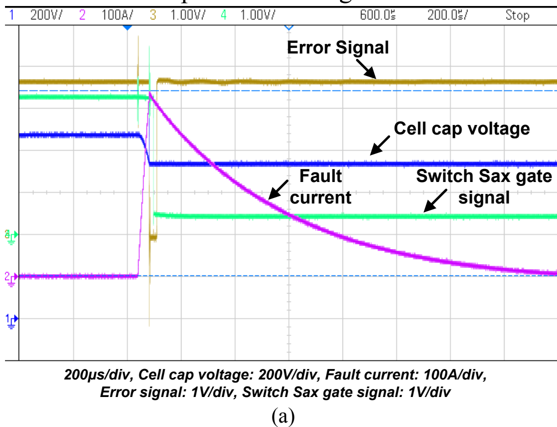
(a)



(b)

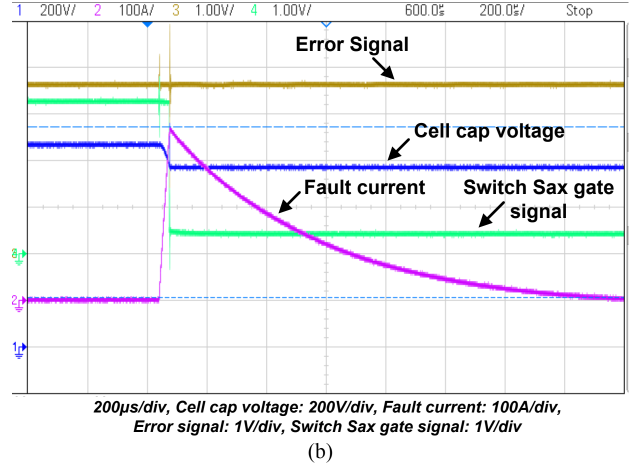
Fig.9: Three dimensional plot for threshold setting against actual tripping current for both IGBT protection methods (a) working separately, (b) working simultaneously.

Fig.10 shows experimental results for the test performed with both methods of IGBT protection. Fig.10(a) illustrates the result for driver level protection tripping first (corresponding to point 1 in Fig.9(b)). Driver is set to trip at V_{CE}=6.1V which according to manufacturer datasheet corresponds to I_c=335A. Overcurrent threshold is set to 400A. Fault is triggered when current starts rising. Current continuously rises until driver level protection is triggered by monitoring V_{CE}. An active low error signal flags enabling switch Sax to trip open hence tripping the IGBT at peak trip current 440A. Cell capacitor voltage (initially at 900V) starts reducing as the discharge current builds up and is held constant at 720V once switch *Sax* trips open. The error signal is reset by microcontroller ready for the next trip. Fig.10(b) shows the case corresponding to point 2 in Fig.9(b). Driver is set to trip at the same V_{CE}=6.1V which according to manufacturer datasheet corresponds to I_c=335A. Overcurrent threshold is set to 200A. It can be seen that driver error signal is not activated meaning that IGBT tripping has occurred due to overcurrent feedback control. This is confirmed by the fact the cell capacitor has not fully discharged which means that switch Sax is tripped open at the instant of peak current. Peak current is 373A. Cell capacitor voltage drops to 760V which is marginally higher than the previous case due to the lower peak tripping current which leads to less capacitor discharge.



200μs/div, Cell cap voltage: 200V/div, Fault current: 100A/div, Error signal: 1V/div, Switch Sax gate signal: 1V/div

(a)



200μs/div, Cell cap voltage: 200V/div, Fault current: 100A/div, Error signal: 1V/div, Switch Sax gate signal: 1V/div

(b)

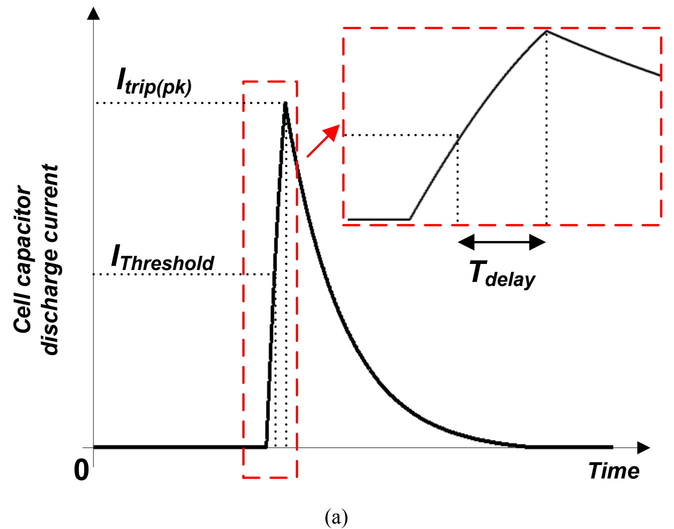
Fig.10: Experimental results for cell capacitor discharge during DC side fault (a) driver level protection triggered, (b) overcurrent protection triggered.

Fig.11(a) illustrates the concept of the delay time T_{delay} causing actual IGBT tripping current to be higher than overcurrent threshold setting. This time delay is made up of two main components; variable (T_{var}) and fixed (T_{fix}) time delay, such that

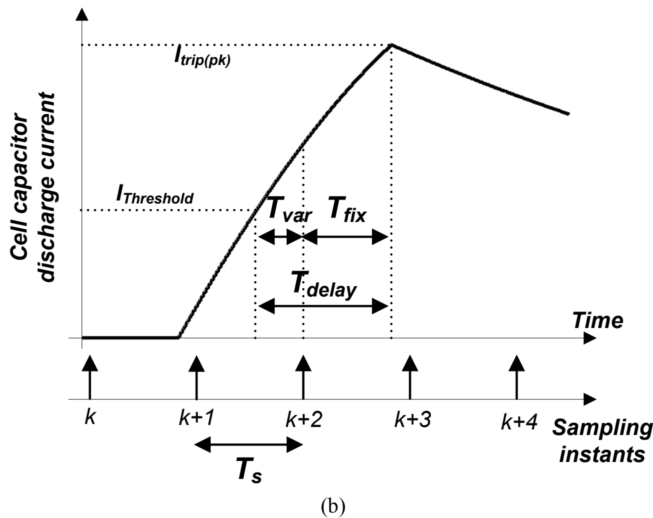
$$T_{delay} = T_{\text{var}} + T_{fix} \tag{15}$$

The fixed time delay can be defined as that from the sensor lag and the circuit propagation delay, and the variable delay is that from microcontroller sampling. This concept is detailed in Fig.11(b). At sampling instant (k+1), the microcontroller does not read an overcurrent. It is not until the next sampling instant (k+2) that the overcurrent is realised which is delayed from its actual occurrence by T_{var}. This time delay is variable since microcontroller sampling is asynchronous with the main circuit. The remaining delay time is the fixed portion T_{fix}. The variable delay time is always in the range of (0 to T_s) and the fixed delay time can be calculated experimentally by recording the maximum achievable $T_{delay(max)}$ and subtracting T_s.

$$T_{fix} = T_{delay(\max)} - T_s \tag{16}$$



(a)



(b)

Fig.11: Illustration of time delay (T_{delay}) concept causing actual tripping current to be higher than threshold setting (a) generic cell capacitor discharge current, (b) detailed view.

4 Conclusion

This paper studied the behaviour of the cell capacitor discharge currents during DC faults in half-bridge modular multilevel converters. Circuit parameter dependent analytical expressions were derived for cell capacitor discharge current slew rate, peak transient current and resultant *I2t* representing thermal energy developed. This included those for the cell main diode and auxiliary switch and accounting for naturally existing switch tripping delays. It was concluded that increasing MMC arm inductance would reduce energy build up in the switches during DC fault, and hence for fault-tolerant MMC configurations, arm inductance can be appropriately selected so as not to over-rate switches for DC faults.

The second part of the paper presented experimental results for discharging 900V MMC capacitor under two levels of switch protection, driver level protection monitoring switch collector-emitter voltage and overcurrent protection with feedback control. It was concluded that driver level protection is generally faster in tripping IGBTs than overcurrent sensing due to the lower aggregate delay times associated with direct hardware protection at device level. Overcurrent sensing can be used to back up driver level protection.

Acknowledgements

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